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Lab 3 Notes

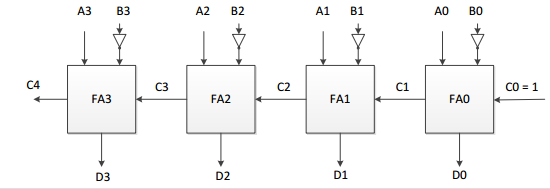
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CSE 2441-001

**Introduction:** Lab 3 introduces the 4 bit full adder subtractor with a carryout function. This circuit is similar to Lab 2 in the essence that it uses 4 1 bit full adders and additionally adds a XOR gate tied to the carry in to produce a two’s complement on bit B to subtract.

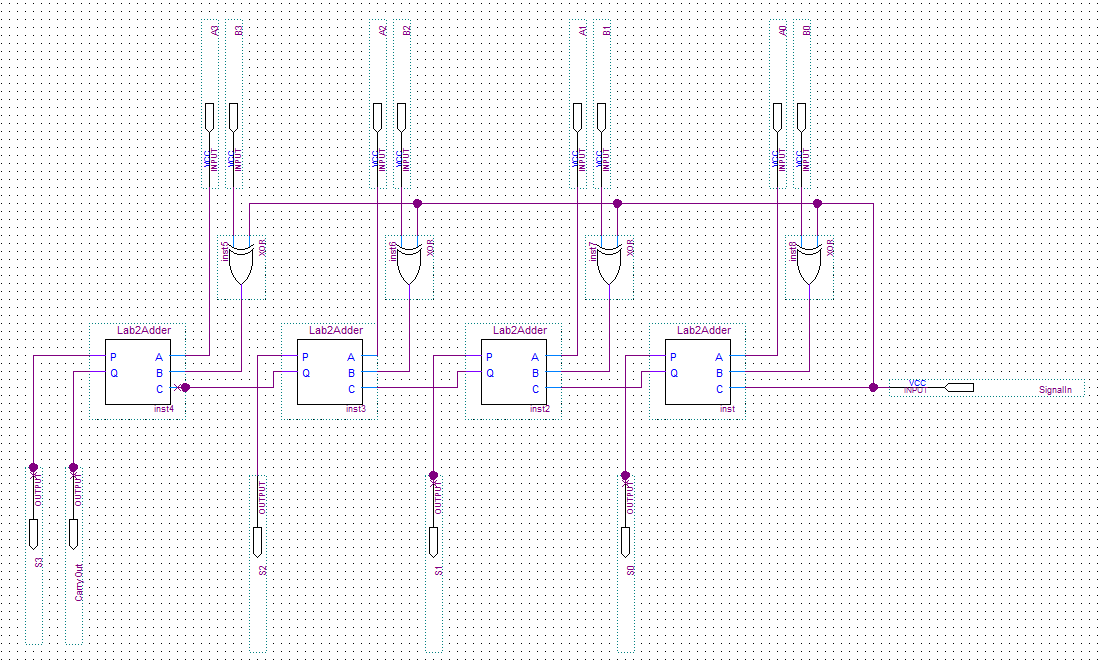
**Theory:** Using 4 1 bit ripple adders along with XOr gates and a carry in as a subtractor signal using two’s complement (Figure 1).

**Figure 1: 4 Bit Ripple Carry adder with XOR circuit and carry in to create subtractor**



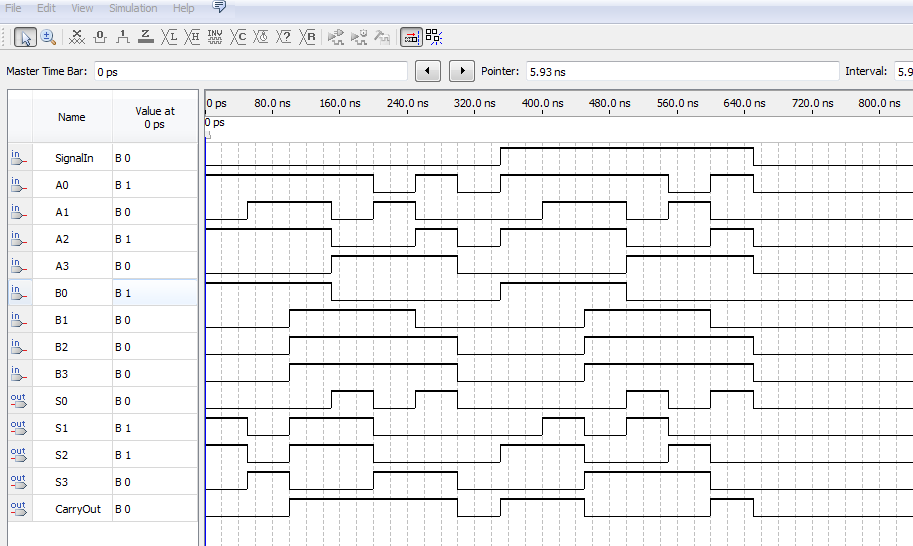
**Procedure:** The design was first implemented in Quartus to verify the design (Figure 2). Next the Adder/Subtractor was wired on a breadboard, finally it was tested on the IDL-800.

**Figure 2: 4 Bit Adder/Subtractor designed in Quartus.**

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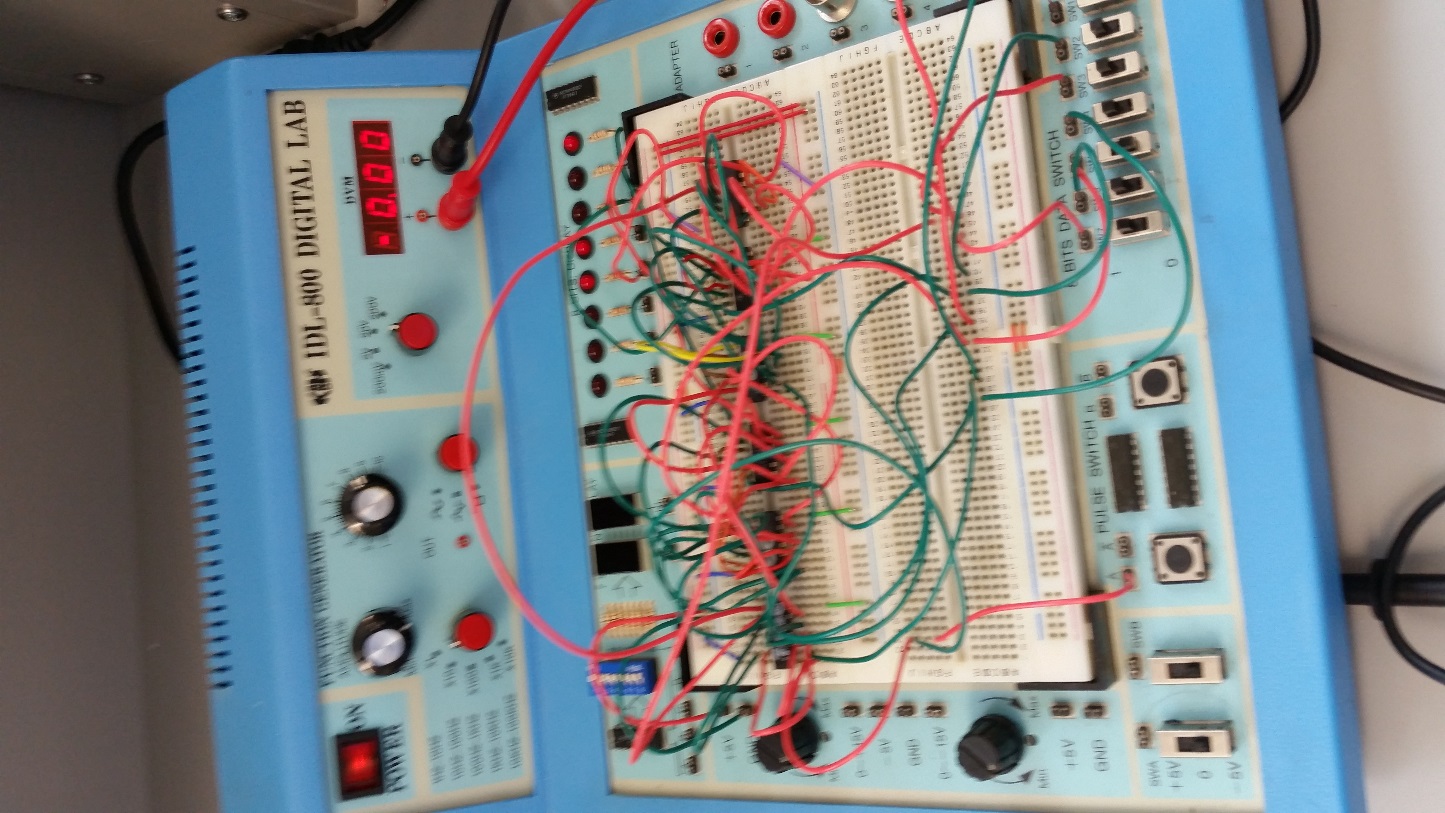
The Adder/Subtractor is then tested using the waveform function in Quartus(Figure 3) to verify correct design. Values given in the Lab write up are used to verify correctness.

**Figure 3: Waveform to verify adder/subtractor design**

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Next the adder/subtractor was implemented using the IDL-800, 2- 7486,2- 7400 chips and the breadboard (Figure 4).

**Figure 4: Implementation of adder/Subtractor**

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The test values were then verified by the lab instructor in the following fashion.

|  |  |  |
| --- | --- | --- |
| *Ripple Carry Adder* | | |
| A | B | S=A+B |
| 0101 | 0001 | 0110 |
| 0111 | 0001 | 1000 |
| 0111 | 1111 | 0110 |
| 1001 | 1110 | 0111 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| *Adder/Subtractor* | | | | | |
| A | B | R=A+B | Cout | R=A-B | Cout |
| 0101 | 0001 | 0110 | 0 | 0100 | 1 |
| 0111 | 0001 | 1000 | 0 | 0110 | 1 |
| 0111 | 1111 | 0110 | 1 | 1000 | 0 |
| 1001 | 1110 | 0111 | 1 | 1011 | 0 |
| 1010 | 1110 | 0111 | 1 | 1100 | 0 |
| 1101 | 1100 | 1001 | 1 | 0001 | 1 |

**Conclusion:** This lab was very tedious as far as wiring was concerned. I predicted this situation and devised a netlist of a pin to pin connection to make wiring faster. This also helped eliminate mistakes and drive troubleshooting if needed. This particular process will help for any future designs. A module was also created in this lab for quick implementation into future designs.